## REMARKS

This is intended as a full and complete response to the Final Office Action dated August 14, 2009, having a shortened statutory period for response set to expire on November 14, 2009. Applicants submit the included amendments with a Request for Continued Examination (RCE). No new matter has been added by those amendments. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-28 are pending in the application. Claims 1-28 remain pending following entry of this response. Claims 1-2 and 9-28 have been amended.

### Rejections under 35 U.S.C. §102(e)

The Examiner rejected claims 1-11 and 13-28 under 35 U.S.C. 102(e) as being anticipated by *Van Hook* (US 6,342,892) (hereinafter *Van Hook*).

As amended, claim 1 recites the limitation of a hardware-based Physics Processing Unit (PPU), comprising a vector processor adapted to perform multiple, parallel floating point operations to generate physics data, where the multiple, parallel floating point operations are specified by a very long instruction word (VLIW) that is issues to the vector processor, and a data communication circuit adapted to communicate the physics data to a host CPU. These amendments are supported by at least page 22, lines 14-16 and page 23, lines 8-10 of the Application, as originally filed. *Van Hook* fails to teach or suggest these claim limitations.

The Examiner analogizes the signal processor 400 of *Van Hook* to be claimed vector processor. See page 3 of the Final Office Action. The Examiner also analogizes the main processor to the claimed host CPU. See page 3 of the Final Office Action. The signal processor 400 of *Van Hook* includes a vector unit 420 that is configured to execute audio and graphics tasks. See *Van Hook*, column 16, lines 7-11.

Applicants disagree with the Examiner's analysis for several reasons. First, Applicants submit that *Van Hook* does not disclose a VLIW that specifies multiple, parallel floating point operations that are performed by a vector processor,as expressly recited in amended claim 1. *Van Hook* teaches only that instructions are

stored in memory and the vector unit is configured to perform the same operation in parallel (see *Van Hook* at col. 18, lines 1-2).

Second, Applicants submit that *Van Hook* does not disclose a vector unit that performs floating point operations. In fact, *Van Hook* actually teaches away from the amended claim 1 since the disclosed vector unit does not perform floating point operations, contrary to what is now claimed. *Van Hook* is clear that "signal processor 400 has no floating point unit" (see col. 18, lines 58-59 of *Van Hook*). Each and every operation performed by the vector unit taught by *Van Hook* must be performed using fixed point operations, not floating point operations. Thus, when the vector unit in *Van Hook* is configured to perform double precision computations, the fixed point format includes a 16 bit integer and a 16 bit fraction (see col. 26, lines 37-51 of *Van Hook*). *Van Hook* does describe that the CPU (main processor) includes a register for floating-point operations. However, as set above, *Van Hook* fails to teach or suggest that the vector unit or any other unit within the PPU (signal processor) is configured to perform floating point operation.

Finally, Applicants submit that *Van Hook* does not disclose a vector unit capable of generating physics data. The disclaimed vector unit 420 receives commands from the main processor interface and executes those commands to process only graphics and audio data (see column 18, lines 1-7 of *Van Hook*). *Van Hook* contains no teachings whatsoever indicating that either the vector unit 420 or the signal processor 400 is capable of generating physics data, as claimed.

As the foregoing illustrates, *Van Hook* fails to teach or suggest each and every limitation of amended claim 1. In particular, *Van Hook* fails to teach or suggest generating physics data and *Van Hook* fails to teach or suggest performing multiple, parallel floating point operations. Therefore, amended claim 1 and claims dependent thereon, are in condition for allowance.

As amended, claim 9 recites also the limitations of a vector processor that is adapted to perform multiple, floating point operations, where the multiple, parallel floating point operations are specified by a very long instruction word (VLIW) that is issued to the vector processor. Therefore, amended claim 9 is allowable for at least

the same reasons as allowable claim 1. Since amended claims 10-11 and 13-28 depend on amended claim 9, these claims are also in condition for allowance.

Rejections under 35 U.S.C. §103(a)

The Examiner rejected claim 12 under 35 U.S.C. 103(a) as being unpatentable over *Van Hook*, as applied to claims 9-11 above, in view of *Intel* (*Intel PCI and PCI Express*; (hereinafter *Intel*). The Examiner relies on *Intel* only to teach the PCI and PCI-Express interfaces, not disclosed in the Van Hook reference. However, as discussed above, Van Hook fails to disclose or suggest several of the limitations now recited in amended claim 9, on which claim 12 depends. Intel fails to cure those deficiencies of Van Hook. Consequently, the combination of Van Hook and Intel cannot now render claim 12 obvious, thereby placing claim 12 in condition for allowance along with the other claims.

**CONCLUSION**

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Final Office Action mailed August 14, 2009 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

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